IN THE CLAIMS

1. (currently amended) A method of making a microelectronic assembly comprising:

providing a first microelectronic element having one or more conductive bumps, said conductive bumps including a first fusible material that transforms from a solid to a liquid at a first melting temperature;

providing a second microelectronic element having one or more conductive elements;

electrically interconnecting said conductive bumps of said first microelectronic element and said conductive elements of said second microelectronic element using a second fusible material, said second fusible material having a second melting temperature that is lower than the first melting temperature of said first fusible material;

during the electrically interconnecting step, maintaining said second fusible material at a temperature that is greater than or equal to the second melting temperature and less than the first melting temperature of said first fusible material; ~~and~~

testing said microelectronic assembly after the electrically interconnecting step while maintaining said second fusible material at a temperature that is greater than or equal to the second melting temperature; and

after the testing step, raising the temperature of the first fusible material to a temperature that is greater than the first melting temperature of said first fusible material for mixing the first and second fusible materials together to form one or more conductive masses.

2. (original) The method as claimed in claim 1, wherein said one or more conductive bumps include C4 bumps.

3. (original) The method as claimed in claim 1, wherein said conductive elements include releasable leads having first ends permanently attached to said second microelectronic element and second ends releasably attached to said second microelectronic element.

4. (canceled)

5. (previously presented) The method as claimed in claim 1, further comprising lowering the temperature of said second fusible material to a temperature that is less than the second melting temperature.

6. (original) The method as claimed in claim 5, wherein the lowering the temperature of said second fusible material follows the electrically interconnecting step.

7. (original) The method as claimed in claim 5, wherein the lowering the temperature of said second fusible material precedes the testing step.

8. (canceled)

9. (currently amended) The method as claimed in claim ~~8~~1, further comprising lowering the temperature of said conductive masses to transform said conductive masses from a liquid state to a solid state, whereupon said first and second microelectronic elements are permanently attached.

10. (original) The method as claimed in claim 1, wherein said first microelectronic element is selected from the group consisting of a semiconductor chip, a semiconductor wafer, a semiconductor chip package having a dielectric element attached to a chip, a circuit board, a dielectric sheet, a circuit panel, a connection component, an interposer, a substrate and a dielectric substrate.

11. (original) The method as claimed in claim 1, wherein said second microelectronic element is selected from the group consisting of a semiconductor chip, a semiconductor wafer,

a semiconductor chip package having a dielectric element attached to a chip, a circuit board, a dielectric sheet, a circuit panel, a connection component, an interposer, a substrate and a dielectric substrate.

12. (original) The method as claimed in claim 1, wherein said second microelectronic element comprises a dielectric layer, the conductive elements being exposed at a first side of the dielectric layer, the dielectric layer having terminals exposed at a second side of the dielectric layer.

13. (original) The method as claimed in claim 12, wherein the conductive elements comprise a plurality of elongated leads extending along the first side of the dielectric layer, each lead having a first end attached to the dielectric layer and a second free end movable away from said dielectric layer.

14. (original) The method as claimed in claim 13, further comprising simultaneously displacing all of the second ends of the leads relative to the first ends of the leads so as to bend the second ends away from the dielectric layer, wherein the displacing step occurs after the first and second microelectronic elements are permanently attached.

15. (original) The method as claimed in claim 14, wherein the leads are curved in shape before the displacing step.

16. (original) The method as claimed in claim 14, wherein the second ends of said leads are releasably secured to said dielectric layer before the displacing step.

17. (original) The method as claimed in claim 14, wherein the step of displacing includes moving said first microelectronic element relative to said dielectric layer.

18. (original) The method as claimed in claim 14, further comprising injecting a flowable dielectric material

between said first and second microelectronic elements after the displacing step and curing the flowable dielectric material to form a dielectric support layer around the leads.

19. (original) The method as claimed in claim 14, further comprising the step of injecting a flowable dielectric material between said first and second microelectronic elements so as to move said first microelectronic element relative to said second microelectronic element.

20. (original) The method as claimed in claim 1, wherein the first microelectronic element comprises a semiconductor wafer including a plurality of semiconductor chips, each said chip including one or more of said conductive bumps.

21. (original) The method as claimed in claim 20, wherein said second microelectronic element includes a flexible dielectric sheet having a top surface and a bottom surface.

22. (original) The method as claimed in claim 21, wherein the conductive elements comprise leads extending along the top surface of the sheet, each of the leads having a first end and a second end, the step of electrically interconnecting including permanently attaching the second ends of said leads to said conductive bumps of said semiconductor wafer.

23. (original) The method as claimed in claim 22, further comprising the step of severing said semiconductor wafer and said flexible dielectric sheet to form individual assemblies including at least one of said semiconductor chips and a region of said dielectric sheet associated therewith.

24. (original) The method as claimed in claim 1, wherein said first microelectronic element includes a semiconductor chip package having at least one semiconductor chip electrically interconnected with a circuitized substrate.

25. (original) The method as claimed in claim 24, wherein said circuitized substrate includes a flexible dielectric element having flexible leads with first ends connected with contacts on said semiconductor chip and second ends remote therefrom, said second ends being electrically interconnected with said conductive bumps including said first fusible material.

26. (original) A method of making a microelectronic assembly comprising:

providing a first microelectronic element having one or more conductive bumps, said conductive bumps including a first fusible material that transforms from a solid to a liquid at a first melting temperature;

providing a second microelectronic element having one or more elongated leads extending along a first side thereof, each lead having a first end attached to said second microelectronic element and a second end remote therefrom;

electrically interconnecting said conductive bumps of said first microelectronic element and the second ends of said elongated leads using a second fusible material, said second fusible material having a second melting temperature that is lower than the first melting temperature of said first fusible material; and

during the electrically interconnecting step, maintaining said second fusible material at a temperature that is greater than or equal to the second melting temperature and less than the first melting temperature of said first fusible material.

27. (original) The method as claimed in claim 26, further comprising testing said microelectronic assembly after the electrically interconnecting step;

28. (original) The method as claimed in claim 27, further comprising lowering the temperature of said second fusible material to a temperature that is less than the second melting temperature.

29. (original) The method as claimed in claim 28, further comprising after the testing step raising the temperature of said first fusible material to a temperature that is greater than the first melting temperature of said first fusible material for mixing said first and second fusible materials to form one or more conductive masses; and

lowering the temperature of said one or more conductive masses to transform said conductive masses from a liquid state to a solid state for permanently attaching said first and second microelectronic elements to one another.

30. (original) The method as claimed in claim 29, further comprising after the permanently attaching step moving the second ends of said leads relative to the first ends of said leads for bending second ends away from said dielectric layer.

31. (original) The method as claimed in claim 30, further comprising injecting a flowable dielectric material between said first microelectronic element and said second microelectronic element after the moving step and curing the flowable dielectric material to form a compliant dielectric layer around said leads.

32. (original) A method of making a microelectronic assembly comprising:

providing a first microelectronic element including one or more contacts;

providing a second microelectronic element including one or more conductive pads and juxtaposing said first and second microelectronic elements with one another so that the one or more contacts face the one or more conductive pads;

forming a releasable electrical interconnection between the contacts of said first microelectronic element and the conductive pads of said second microelectronic element;

testing the assembly while maintaining the releasable electrical interconnection between said first and second microelectronic elements;

after testing, forming a permanent electrical interconnection between said first and second microelectronic elements.

33. (original) The method as claimed in claim 32, wherein the forming a releasable electrical interconnection step includes providing conductive bumps over the contacts of said first microelectronic element, said conductive bumps including a first fusible material that transforms from a solid to a liquid at a first melting temperature.

34. (original) The method as claimed in claim 33, wherein the forming a releasable electrical interconnection further comprises electrically interconnecting said conductive bumps and the conductive pads of said second microelectronic element using a second fusible material having a second melting temperature that is lower than the first melting temperature of said first fusible material.

35. (original) The method as claimed in claim 34, wherein during the forming a releasable electrical interconnection step, said second fusible material is at a temperature that is greater than or equal to the second melting temperature and less than the first melting temperature of said first fusible material.

36. (original) The method as claimed in claim 34, further comprising lowering the temperature of said second fusible material to below the second melting temperature before the testing the assembly step.

37. (original) The method as claimed in claim 34, further comprising, after the testing the assembly step raising the temperature of the first fusible material to above the first melting temperature for mixing said first and second fusible materials together to form one or more conductive masses electrically interconnecting said first and second microelectronic elements.

38. (original) The method as claimed in claim 32, wherein said first microelectronic element is selected from the group consisting of a semiconductor chip, a semiconductor wafer, a semiconductor chip package having a dielectric element attached to a chip, a circuit board, a dielectric sheet, a circuit panel, a connection component, an interposer, a substrate and a dielectric substrate.

39. (original) The method as claimed in claim 32, wherein said second microelectronic element is selected from the group consisting of a semiconductor chip, a semiconductor wafer, a semiconductor chip package having a dielectric element attached to a chip, a circuit board, a dielectric sheet, a circuit panel, a connection component, an interposer, a substrate and a dielectric substrate.

40. (withdrawn) A microelectronic assembly comprising:

a first microelectronic element having a contact bearing face and one or more contacts provided at the contact bearing face;

a second microelectronic element juxtaposed with said first microelectronic element, said second microelectronic element having a first surface including one or more conductive pads;

one or more conductive masses electrically interconnecting the contacts of said first microelectronic

element and the conductive pads of said second microelectronic element, wherein each said conductive mass includes a first region comprising a first fusible material transformable from a solid to a liquid at a first melting temperature and a second region comprising a second fusible material transformable from a solid to a liquid at a second melting temperature that is less than the first melting temperature.

41. (withdrawn) The microelectronic assembly of claim 40, further comprising substantially S-shaped leads having tip ends that are electrically connected to the contacts of said first microelectronic element and terminal ends that are permanently attached to the conductive pads of said second microelectronic element.

42. (withdrawn) The microelectronic assembly as claimed in claim 40, wherein the first region of each said conductive mass includes a conductive bump attached to one of the contacts of said first microelectronic element.

43. (withdrawn) The microelectronic assembly as claimed in claim 42, wherein the second region of each said conductive mass includes a layer of a fusible conductive material interposed between one of the conductive bumps of said first microelectronic element and one of the conductive pads of said second microelectronic element.

44. (withdrawn) The microelectronic assembly as claimed in claim 40, wherein said first microelectronic element is selected from the group consisting of a semiconductor chip, a semiconductor wafer, a semiconductor chip package having a dielectric element attached to a chip, a circuit board, a dielectric sheet, a circuit panel, a connection component, an interposer, a substrate and a dielectric substrate.

45. (withdrawn) The microelectronic assembly as claimed in claim 40, wherein said second microelectronic

assembly is selected from the group consisting of a semiconductor chip, a semiconductor wafer, a semiconductor chip package having a dielectric element attached to a chip, a circuit board, a dielectric sheet, a circuit panel, a connection component, an interposer, a substrate and a dielectric substrate.

46. (withdrawn) The microelectronic assembly as claimed in claim 40, wherein said first microelectronic element includes a semiconductor wafer comprising a plurality of semiconductor chips, said wafer being severable for providing individual packages comprising one or more of said semiconductor chips electrically interconnected with at least a region of said second microelectronic element.

47. (withdrawn) The microelectronic assembly as claimed in claim 40, further comprising an array of flexible leads extending between and electrically interconnecting said first and second microelectronic elements.